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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,497	04/16/2004	Yoo-Sok Saw	2060-3115	1342

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EXAMINER	
LAI, DANIEL	
ART UNIT	PAPER NUMBER
2617	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,497	SAW, YOO-SOK	
	Examiner	Art Unit	
	Daniel Lai	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/826,497.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 6-11, 16-24 and 26 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art (Admission).

3. Regarding claim 1, Applicant discloses in Description of the Related Art of the instant applicant a related art TDD apparatus comprising:

a receiving unit for receiving and converting an RF signal (paragraph 7);

a processing unit for recognizing a construction of uplink time slots and downlink time slots from the converted RF signal (paragraph 9 and 10);

a detecting unit for detecting a switching point from the converted RF signal and determining a new switching point based on the detected switching point and the recognized construction of uplink time slots and downlink time slots (paragraph 19 (the modem 10 determines a switching time of the TDD switch 40, taking into consideration a signal processing delay time defined by the communication system));

a transmitting unit for transmitting a data signal (paragraph 7); and

a switching unit for switching between the receiving unit and the transmitting unit according to the switching point (paragraph 12).

4. Regarding claim 6, the admitted prior art discloses the detecting unit (modem 10) controls the switching unit to switch between the receiving unit and the transmitting unit (paragraph 12).

5. Regarding claim 7, the admitted prior art discloses the detecting unit determines the switching point based on an actual signal processing time of the transmitting unit (paragraphs 10-11).

6. Regarding claims 8 and 9, the admitted prior art discloses a software-based modem and a hardware-based modem (paragraphs 13, 14).

7. Regarding claim 10, the admitted prior art discloses the apparatus is TDD-based (paragraph 6).

8. Regarding claims 11 and 21, the admitted prior art discloses an apparatus and method for synchronizing uplink and downlink comprising:

a receiver adapted to convert a received RF downlink signal to a digital signal (paragraph 7);

a modem adapted to examine the digital signal to recognize a construction of uplink time slots and downlink time slots and to generate time slot construction information (paragraph 9 and 10);

a time slot detector adapted to examine the digital signal to detect a first switching point between uplink time slots and downlink time slots and to determine a second switching point based on the detected first switching point and time sot construction information (paragraph 19 (the modem 10 determines a switching time of the TDD

switch 40, taking into consideration a signal processing delay time defined by the communication system));

an RF transmitter adapted to transmit an uplink data signal (paragraph 7); and

a TDD switch adapted to switch between the receiver and transmitter according to the second switching point (paragraph 12).

9. Regarding claim 16, the admitted prior art discloses the detecting unit (modem 10) controls the switching unit to switch between the receiving unit and the transmitting unit (paragraph 12).

10. Regarding claim 17, the admitted prior art discloses the detecting unit determines the switching point based on an actual signal processing time of the transmitting unit (paragraphs 10-11).

11. Regarding claims 18 and 19, the admitted prior art discloses a software-based modem and a hardware-based modem (paragraphs 13, 14).

12. Regarding claim 20, the admitted prior art discloses the apparatus is TDD-based.

13. Regarding claim 22, the admitted prior art discloses the method further comprising the step of :

delaying a transmitted data signal such that a transmission point of the data signal corresponds to a switching point for uplink transmission (paragraphs 10-12, where modem detects a new switching point and then transmits a transmission signal to the transmitter for uplink transmission).

14. Regarding claim 23, the admitted prior art discloses wherein the step of delaying the transmitted data signal further comprises selecting a data signal to be delayed and adjusting a

delay time of the signal (paragraph 12). Modem 10 controls the switching time of TDD switch 40 for the transmitting data signal corresponding to the determined switching point.

15. Regarding claim 24, the admitted prior art discloses the recognition of a construction of uplink time slots and downlink times slots is performed by a software modem (paragraph 13).

16. Regarding claim 26, the admitted prior art discloses determining a second switching point comprises based on an actual signal processing time of the transmitting unit (paragraph 10,11).

Claim Rejections - 35 USC § 103

17. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

18. Claims 2-5, 12-15 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (Admission) in view of Wildey (US 6,463,080).

19. Regarding claim 2, the admitted prior art discloses the limitations of claim 1 as applied above. The reference further discloses the delay is fixed (paragraph 11, where the processing delay time is a fixed value). The reference fails to disclose the delay is variable. Wildey teaches an apparatus with variable delay and by inserting such a variable delay can improve communication quality (col. 2, line 63-col. 3, line 10; col. 6, line 34-48). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the synchronizing terminal as disclosed by the admitted prior art with the variable delay taught by

Wildey such that the synchronizing terminal can introduce variable delay instead of a fixed delay to the signal to enhance communication quality.

20. Regarding claim 3, the admitted prior art discloses the modem 10 controls the transmitting unit to delay the transmitted data signal with the corresponding determined switching point (paragraphs 10-12).

21. Regarding claim 4, the admitted prior art discloses the transmitting units selects a data signal to be delayed and adjusts a delay time of the signal (paragraph 12).

22. Regarding claim 5, the admitted prior art discloses the limitations of claim 1 as applied above. The reference further discloses the delay is fixed (paragraph 11, where the processing delay time is a fixed value). The reference fails to disclose the delay is variable. Wildey teaches an apparatus with variable delay and by inserting such a variable delay can improve communication quality (abstract; col. 2, line 63-col. 3, line 10; col. 6, line 34-48). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the synchronizing terminal as disclosed by the admitted prior art with the variable delay taught by Wildey such that the synchronizing terminal can introduce variable delay instead of a fixed delay to the signal to enhance communication quality.

23. Regarding claim 12, the admitted prior art discloses the limitations of claim 11 as applied above. The reference further discloses the delay is fixed (paragraph 11, where the processing delay time is a fixed value). The reference in additionally discloses the modem 10 determines a new switching point and controls the switch 40 according to the determined switching point (paragraphs 10-12). Therefore, there is a delay unit to delay the switching time. The reference fails to disclose a variable delay unit. Wildey teaches an apparatus comprises a time delay

controller that varies delay (variable delay unit) and Wildey teaches that using such a time delay controller can improve communication quality (abstract; col. 2, line 63-col. 3, line 10; col. 6, line 34-48). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the synchronizing terminal as disclosed by the admitted prior art with the time delay controller as taught by Wildey such that the synchronizing terminal can introduce variable delay instead of a fixed delay to the signal to improve communication quality.

24. Regarding claim 13, the admitted prior art teaches the modem 10 determines a new switching point and controls the switch 40 according to the determined switching point (paragraphs 10-12). Therefore, the delay unit is controlled by the modem to use the determined switching point to control the switch.

25. Regarding claim 14, the admitted prior art discloses many of the limitations of claim 12 as applied above. The reference fails to disclose the variable delay unit is adapted to select a data signal to be delayed and to adjust a delay time of the signal. Wildey teaches the time delay controller select demodulated signal and applies delay to the signal (col. 6, line 49-56). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the synchronizing terminal as disclosed by the admitted prior art with the time delay controller taught by Wildey such that the synchronizing terminal can introduce a variable delay to the signal and hence communication quality is increased.

26. Regarding claims 15 and 25, the admitted prior art discloses the limitations of claims 11 and 21 as applied above. The reference further discloses that that TDD switch is adapted to switch at a fixed time interval according to the determined switching point (paragraphs 10-11, where the processing delay time is a fixed value). The reference fails to disclose the delay is

variable. Wildey teaches using variable delay for the signal and by inserting such a variable delay can increase communication quality (col. 2, line 63-col. 3, line 10; col. 6, line 34-48). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the synchronizing terminal as disclosed by the admitted prior art with the variable delay taught by Wildey such that the synchronizing terminal can introduce variable delay instead of a fixed delay to the signal to enhance communication quality.

27. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Riley (US 6,072,783).

28. The Applicant's admitted prior art discloses the limitations of claim 21 as applied above. The reference lacks counting the number of uplink and downlink time slots in the overall time slots of an uplink/downlink channel. Riley teaches method to control systems using data link modules comprises counting the number of time slots in each frame of the master clock (col. 6, line 6-7) to provide provision of a data link (col. 6, line 1-2). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the synchronization apparatus as disclosed by the admitted prior art and the method to count the number of time slot taught by Riley so that data link provision can be provided to the synchronization apparatus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Lai whose telephone number is (571) 270-1208. The examiner can normally be reached on Monday – Thursday, 9:00 a.m. – 4:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nick Corsaro can be reached on (571) 272-7876. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DL D.L.

Nick Corsaro

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